IN THE CLAIMS

1. (Original) A circuit for amplifying signals, the circuit comprising:

a control line; and

a two terminal semiconductor device having first and second terminals, the first terminal coupled to a signal line, and the second terminal coupled to the control line, wherein the two terminal semiconductor device is adapted to have a capacitance when a voltage on the first terminal relative to the second terminal is above a threshold voltage and to have a lower capacitance when the voltage on the first terminal relative to the second terminal is less than the threshold voltage,

wherein the control line is adapted to be coupled to a control signal and wherein the signal line is adapted to be coupled to a signal and to be an output of the circuit.

2. (Original) The circuit of claim 1, wherein the two terminal semiconductor device comprises a gated diode having a well and wherein the threshold voltage can be modified by modifying a dopant level in the well of the gated diode.

3. (Original) The circuit of claim 1, further comprising an isolation device intermediate the signal line and the two terminal semiconductor device, the isolation device having an input, an output and a control terminal, the input of the isolation device coupled to the signal line and the output of the isolation device coupled to the first terminal, wherein the output of the isolation device is adapted to be the output of the circuit, and whereby the control terminal of the isolation device can be set to a control voltage.

4. (Amended) The circuit of claim 3, wherein the isolation device is adapted:

to isolate the signal on the signal line from the first terminal of the two terminal semiconductor device when a voltage on the first terminal of the two terminal semiconductor device is greater than a predetermined voltage and a control voltage on the control terminal of the isolation device is set to ~~the~~ a predetermined control voltage; and

to pass the signal on the signal line from the first terminal of the two terminal semiconductor device when a voltage on the first terminal of the two terminal semiconductor device is less than a predetermined voltage and a control voltage on the control terminal of the isolation device is set to the predetermined control voltage.

5. (Original) The circuit of claim 3, wherein the isolation device comprises a Field Effect Transistor (FET).

6. (Amended) The circuit of claim 5, wherein the isolation device is adapted:

to be turned off when a voltage on the first terminal of the two terminal semiconductor device is greater than a predetermined voltage and a control voltage on the control terminal of the isolation device is set to ~~the~~ a predetermined control voltage; and

to be turned on when a voltage on the first terminal of the two terminal semiconductor device is less than a predetermined voltage and a control voltage on the control terminal of the isolation device is set to the predetermined control voltage.

7. (Original) The circuit of claim 5, wherein the FET is an n-type FET.

8. (Original) The circuit of claim 5, wherein the FET is a p-type FET.

9. (Original) The circuit of claim 1, further comprising an output circuit adapted to produce an output corresponding to a voltage at the gate input of the gated diode.

10. (Original) The circuit of claim 9, wherein the output circuit comprises one or more of the following: a buffer, an inverter, and a latch.

11. (Original) The circuit of claim 1, wherein the two terminal semiconductor device comprises a gated diode comprising an insulator formed between a gate and a well, a source diffusion region abutting and overlapping one side of the insulator and gate, and a shallow trench isolation region abutting another side of the insulator and gate,

wherein the second terminal is coupled to the source diffusion region and the first terminal is coupled to the gate.

12. (Original) The circuit of claim 1, wherein the two terminal semiconductor device comprises a gated diode comprising an insulator formed between a gate and a well, a source diffusion region abutting and overlapping one side of the insulator and gate, a drain diffusion region abutting and overlapping another side of the insulator and gate, and a coupling that electronically couples the source and drain regions, wherein the second terminal is coupled to the source diffusion region and the first terminal is coupled to the gate.

13. (Original) The circuit of claim 1, wherein the two terminal semiconductor device comprises a gated diode.

14. (Original) The circuit of claim 13, wherein the gated diode is an n-type gated diode, wherein the threshold voltage is a positive voltage, wherein the two terminal semiconductor device is adapted to have a capacitance when a voltage on the first terminal relative to the second terminal is more positive than the threshold voltage and to have a lower capacitance when the voltage on the first terminal is less positive than the threshold voltage.

15. (Original) The circuit of claim 13, wherein the gated diode is a p-type gated diode, wherein the threshold voltage is a negative voltage, wherein the two terminal semiconductor device is adapted to have a capacitance when a voltage on the first terminal relative to the second terminal is more negative than the threshold voltage and to have a lower capacitance when the voltage on the first terminal is less negative than the threshold voltage.

16. (Original) The circuit of claim 1, wherein the output is a first output and wherein the circuit further comprises:

a second control line;

a second two terminal device having an additional first terminal and an additional second terminal, the second first terminal coupled to a second signal line, and the additional second terminal coupled to the second control line, wherein the second control line is adapted to be coupled to the control signal and wherein the second signal line is adapted to be coupled to a second signal and to be a second output, wherein the second two terminal semiconductor device is adapted to have a capacitance when a voltage on the first terminal is above a threshold voltage and to have a lower capacitance when the voltage on the first terminal is less than the threshold voltage; and

a differential signal circuit coupled to the first and second outputs and adapted to output at least one voltage corresponding to the first and second outputs.

17. (Original) The circuit of claim 3, further comprising:

a control voltage generator coupled to the control terminal of the isolation device and adapted to produce and adjust the control voltage.

18. (Original) The circuit of claim 17, wherein the control voltage generator comprises a reference voltage generating circuit producing at least a reference voltage and a voltage output circuit producing the control voltage, the voltage output circuit having inputs of at least the control voltage and the reference voltage.

19. (Original) The circuit of claim 18, wherein the reference voltage generating circuit further produces a digital voltage coupled to the voltage output circuit.

20. (Original) The circuit of claim 18, wherein the reference voltage generating circuit is coupled to one or more of the following inputs: a ground voltage; a power supply voltage; the input signal; the threshold voltage; one or more additional threshold voltages; one or more temperature signals; and the control voltage.

21. (Original) A method for amplifying signals, the method comprising the steps of:

determining that a voltage on a signal line is to be amplified; and

modifying voltage on a control line, wherein the control line is coupled to a second terminal of a two terminal semiconductor device, the two terminal semiconductor device having the second terminal and a first terminal, the first terminal coupled to the signal line, the second terminal coupled to the control line, wherein the two terminal semiconductor device is adapted to have a capacitance when a voltage on the first terminal is above a threshold voltage and to have a lower capacitance when the voltage on the first terminal is less than the threshold voltage, and wherein the control line is adapted to be coupled to a control signal and wherein the signal line is adapted to be coupled to a signal and to be an output of the circuit.

22. (Original) The method of claim 21, further comprising the step of determining a sensed voltage based on a voltage at the output, whereby the sensed voltage will be amplified when a voltage on the first terminal relative to the second terminal is above the threshold voltage and will not be amplified when a voltage on the first terminal relative to the second terminal is below the threshold voltage.

23. (Original) The method of claim 21, wherein the two terminal semiconductor device comprises a gated diode having a well and wherein the threshold voltage can be modified by modifying a dopant level in the well of the gated diode.

24. (Original) The method of claim 21, wherein an isolation device is intermediate the signal line and the two terminal semiconductor device, the isolation device having an input, an output and a control terminal, the input of the isolation device coupled to the signal line and the output of the isolation device coupled to the first terminal, wherein the output of the isolation device is adapted to be the output of the circuit, and wherein the method further comprises the step of applying a control voltage to the control terminal of the isolation device, the control voltage being greater than a threshold voltage of the isolation device.

25. (Original) The method of claim 24, wherein the control voltage applied to the control terminal of the isolation device plus an expected voltage for a signal coupled

to the input of the isolation device, whereby the isolation device passes signals having voltages less than the expected voltage and does not pass signals having voltages greater than the expected voltage.

26. (Original) The method of claim 24, wherein the isolation device comprises a Field Effect Transistor (FET) and wherein the FET is adapted to be turned on when voltage on the signal line is below a predetermined value, and is adapted to be turned off when voltage on the first terminal of the two terminal semiconductor device is above a predetermined value.

27. (Original) The method of claim 26, wherein the FET is an n-type FET, wherein the control terminal of the FET is the gate of the FET, and wherein the step of applying a control voltage to the control terminal of the isolation device of the isolation device further comprises the step of applying a voltage above a threshold voltage to the gate of the FET.

28. (Amended) The method of claim 26, wherein the FET is a p-type FET, wherein the control terminal of the FET is a gate, and wherein the step of applying a control voltage to the control terminal of the isolation device of the isolation device further comprises the step of applying a voltage below a threshold voltage to the gate of the FET.

29. (Original) The method of claim 21, wherein the two terminal semiconductor device comprises a gated diode comprising an insulator formed between a gate and a well, a source diffusion region abutting and overlapping one side of the insulator and gate, and a shallow trench isolation region abutting another side of the insulator and gate, wherein the second terminal is coupled to the source diffusion region and the first terminal is coupled to the gate.

30. (Original) The method of claim 21, wherein the two terminal semiconductor device comprises a gated diode comprising an insulator formed between a

gate and a well, a source diffusion region abutting and overlapping one side of the insulator and gate, a "drain" diffusion region abutting and overlapping another side of the insulator and gate, and a coupling that electronically couples the source and "drain" regions, wherein the second terminal is coupled to the source diffusion region and the first terminal is coupled to the gate.

31. (Original) The method of claim 21, wherein the two terminal device comprises a gated diode.

32. (Original) The method of claim 31, wherein the gated diode further comprises an n-type gated diode, wherein the threshold voltage is a positive voltage and wherein the step of modifying voltage on a control line comprises the step of raising voltage from about ground to a predetermined positive voltage.

33. (Original) The method of claim 31, wherein the gated diode further comprises an p-type gated diode, wherein the threshold voltage is a negative voltage and wherein the step of modifying voltage on a control line comprises the step of lowering voltage from about a power supply voltage to a predetermined positive voltage.

34. (Original) The method of claim 33, wherein the predetermined positive voltage is between ground and the supply voltage.

35. (Original) The method of claim 21, wherein the method further comprises the step of determining an output corresponding to the signal.

36. (Original) The method of claim 24, further comprising the step of generating the control voltage by using at least a reference voltage and the control voltage.

37. (Original) The method of claim 36., wherein the step of generating the control voltage further comprises the step of generating the reference voltage by using

one or more of the following: a ground voltage; a power supply voltage; the signal; the threshold voltage; one or more additional threshold voltages; one or more temperature signals; and the control voltage.

38. (Original) A semiconductor device comprising:

a gate;

a well having a first conductivity type;

an insulator formed between the gate and the well;

a source diffusion region of a second conductivity type abutting and overlapping one side of the insulator and gate; and

an isolation region abutting another side of the insulator and gate.

39. (Original) The semiconductor device of claim 38., wherein the first conductivity type comprises an n-type conductivity and the second conductivity comprises a p-type conductivity.

40. (Original) The semiconductor device of claim 38, wherein the first conductivity type comprises a p-type conductivity and the second conductivity comprises an n-type conductivity.

41. (Original) The semiconductor device of claim 38, wherein the well is formed in a substrate.

42. (Original) The semiconductor device of claim 38, wherein the well is formed in a layer formed above an insulator.